**In the Specification:**

Please amend page 1 under "Priority Claim" as follows:

The present application claims priority from French Application for Patent No. 02 09615 filed July 29, 2002~~, the disclosure of which is hereby incorporated by reference~~.

Please amend Paragraph [10] as follows:

[10] The present invention proposes a device for the adjustment of an operating parameter of an analog electronic circuit. A set of adjustment resistances can be configured from outside the circuit to modulate the value of resistances in the circuit and thus adjust the value of the said parameter. Fusible means are ~~provide~~ provided associated with one of the said adjustment resistances and that will be selected and activated to configure the resistances of the adjustment device.

Please amend Paragraph [19] as follows:

[19] According to one advantageous embodiment, it comprises means ~~of~~ for adjusting a breakdown voltage threshold of the fusible elements.

Please amend Paragraph [20] as follows:

[20] For example, these adjustment means may comprise a resistance bridge arranged between the gate ~~grid~~ and the source and between the gate ~~grid~~ and the drain of each MOS transistor.

Please amend Paragraph [50] as follows:

[50] Concerning the network of diodes T1 to T7 in the first stage 24, they are connected to the cathode C and to the ground through a resistance R3. The two-pole transistor T6 forming one of the diodes in the diodes network is connected to a gate ~~grid~~ G of a transistor M1 through a first hysteresis circuit 30, the drain D of this MOS transistor M1 outputting the clock signal H through a second hysteresis circuit 32.

Please amend Paragraph [51] as follows:

[51] Similarly, diodes T8 to T11 in the second stage 26 are connected firstly to the cathode C and secondly to the ground through a resistance R4. The common terminal between the transistor T11 and the resistance R4 is connected to the gate ~~grid~~ G of a MOS transistor M2. The drain D of this MOS transistor M2 is connected to a node U2, which outputs the threshold voltage UVLO2 through an inverter gate 28.

Please amend Paragraph [53] as follows:

[53] When the power supply voltage applied to the cathode C is less than the threshold voltage UVLO2, the network of diodes composed of transistors T8 to T11 is blocked. The transistor gate ~~grid~~ M2 is then connected to the ground through the resistance R4. The voltage of node U2 is then at a high level, and the output from the inverter gate 28 is at a low level. This voltage then controls the count circuit 16 through an appropriate conventional type of stage, so as to reset the counters in the circuit to 0. The adjustment device is then inactive. For a power supply voltage greater than the threshold voltage UVLO2, the diodes composed of transistors T8 to T11 are conducting. The MOS transistor M2 that operates under saturated conditions, connects node U2 to the ground. The device is then active and the reference voltage source is deactivated.

Please amend Paragraph [54] as follows:

[54] Furthermore, when the power supply voltage output to the cathode C is less than the voltage level UVLO1, the diodes formed by transistors T1 to T7 are not conducting. The gate ~~grid~~ G of transistor M1 is made high through a MOS transistor M3 placed between the cathode and the anode, the gate ~~grid~~ of which is connected to the common node between the transistor T7 and the resistance R3 and that operates under non-conducting conditions. The node U1 is then set to a high level.

Please amend Paragraph [60] as follows:

[60] This circuit 32 comprises a MOS transistor M5, the source S of which is connected to the cathode C and the drain of which is connected to the MOS transistor M1. An inverter switch 36 is connected to the drain of the transistor M5 and outputs the clock signal H. The gate ~~grid~~ of the transistor M5 is connected to the output from the inverter switch 36.